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EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2671	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,006	KIRK ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: According to MPEP § 608.01 (m), the present Office practice is to insist that each claim must be the object of a sentence starting with "I (or we) claim," "The invention claimed is" (or the equivalent). The phrase "Claims" is not considered equivalent to these appropriate phrases. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 7 and 21-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Duluk 1 (US006288730B1).

4. With regard to Claim 7, Duluk 1 describes a method for processing fragments under control of a fragment program in a fragment processing unit (OpenGL, Col. 5, lines 25-31; *texture unit 1200 receives texture coordinates for individual fragments, generates a texture value for each fragment*, Col. 8, lines 11-14), comprising determining a write to a location in a buffer

is pending prior to reading the location in the buffer; waiting for the write complete (*for each memory address received as a request on bus 2601, conflict detection block 2602 determines if a memory conflict is likely to occur*, Col. 14, lines 18-21; *if a conflict is determined by conflict detection block 2602, the conflicting address request is sent to conflict queue 2604*, Col. 14, lines 24-27); reading the location in the buffer; and processing a fragment in the fragment processing unit as specified by the fragment program (*texture memory management unit (MMU) 1210 controls access to texture memory 1213, MMC access from texel prefetch buffer 1216, a variety of locations are available for texture addresses to be received, after the texels for a given fragment are retrieved, texture interpolator 1218 interpolates the texel color values to generate a color value for the fragment, the color value is sent down the pipeline to a shading block*; Col. 8, line 59-Col. 9, line 13).

5. With regard to Claim 21, Duluk 1 describes a system for processing fragments (Col. 8, lines 11-14), comprising means for determining whether a position conflict exists for a fragment, prior to processing the fragment. If a conflict is determined, the conflicting address request is sent to conflict queue 2604 (Col. 14, lines 24-27), meaning that the memory access is deferred until the position conflict does not exist. When the position conflict does not exist, the memory access is allowed, and the processing of a fragment occurs (Col. 9, lines 2-13).

6. With regard to Claim 22, Duluk 1 describes that the processing includes shading (Col. 8, lines 14-18).

7. With regard to Claim 23, Duluk 1 describes that the memory system can service requests while the texture unit is working on hit data, thus minimizing stalls (Col. 10, lines 48-52). Therefore, while the texture unit is working on hit data, which is a fragment for which a position conflict exists (Col. 14, lines 18-21, 24-27; Col. 9, lines 2-12), a fragment for which a position conflict does not exist can be serviced, which means that a fragment for which a position conflict does not exist to bypasses a fragment for which a position does exist.

8. With regard to Claim 24, Duluk 1 describes that for each memory address received as a request on bus 2601, conflict detection block 2602 determines if a memory conflict is likely to occur based upon the address contained in first level reorder queue 2603, meaning that the first level reorder queue 2603 stores at least a portion of a position associated with a fragment (Col. 14, lines 12-40; Col. 9, lines 2-13).

9. With regard to Claim 25, Duluk 1 describes that for each memory address received as a request on bus 2601, conflict detection block 2602 determines if a memory conflict is likely to occur based upon the address contained in first level reorder queue 2603, meaning that the first level reorder queue 2603 stores data corresponding to a region including a position associated with a fragment (Col. 14, lines 12-40; Col. 9, lines 2-13).

10. Thus, it reasonably appears that Duluk 1 describes or discloses every element of Claims 7 and 21-25 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. Claims 1, 4, and 12-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Duluk 1 (US006288730B1) in view of Duluk 2 (US006771264B1).

14. With regard to Claim 1, Duluk 1 describes a method of processing graphics data using a buffer (1216, Figure 2) comprising receiving fragments, a fragment associated with a location in the buffer (Col. 8, lines 19-51); tracking a pending write to the location in the buffer (Col. 14, lines 19-24); shading at least a portion of the fragments to produce shaded fragment data (Col. 8, lines 14-18). For additional shading operations, the operation first waits to read the location in the buffer until the pending write to the location in the buffer is completed (Col. 14, lines 24-27).

After it is completed, the buffer access is allowed, so then the shading block shades the fragment using data read from the location in the buffer to produce additional shaded fragment data (Col. 8, lines 14-18).

However, Duluk 1 does not teach specifically teach writing the shaded fragment data to at least one location in the buffer; and writing the additional shaded fragment data to a location in the buffer. However, Duluk 2, which is a related patent, describes writing the shaded fragment data (*performs phong shading for each pixel fragment*, Col. 44, lines 51-61) to at least one location in the buffer (*BKE bus writes into the frame buffer memory*, Col. 112, line 64-Col. 113, line 4), as shown in Figure 9. This is done for every shaded fragment, so it includes writing the additional shaded fragment data to a location in the buffer.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Duluk 1 to include writing the shaded fragment data to at least one location in the buffer; and writing the additional shaded fragment data to a location in the buffer as suggested by Duluk 2 because Duluk 2 suggests that the shaded fragment data must be stored in a buffer so that it can be scanned out for display (Col. 112, line 64-Col. 113, line 4).

15. With regard to Claim 4, Duluk 1 describes that data stored in the location in the buffer is also stored in an entry in a data cache (*when texels are moved into texel prefetch buffer 1216, a corresponding tag is created in one of the eight prefetch buffer tag blocks 1220-0 through 1220-7*, Col. 12, lines 3-7, *this mapping ensures that all eight tags can be accessed in each cycle, and that texture information is evenly distributed in the caches*, Col. 12, lines 35-37).

16. With regard to Claim 12, Duluk 1 describes a programmable graphics processor (*texture memory address data structure 1280 is also programmable*, Col. 11, lines 64-65) for executing of program instructions comprising a conflict detection unit (2602, Figure 13b) configured to selectively store at least a portion of a position associated with a fragment and generate a position conflict status (Col. 14, lines 18-21); a read interface (1210, Figure 2) configured to read data associated with the position from a graphics memory and output the data to a fragment processing unit (1218; *MMU 1210 controls access to texture memory 1213*, Col. 8, lines 59-60; Col. 9, lines 2-13); the fragment processing unit configured to receive a fragment associated with the position, and the data from the read interface and generate a processed fragment (Col. 9, lines 2-13).

However, Duluk 1 does not specifically teach a write interface configured to write the processed fragment to the graphics memory. However, Duluk 2 describes a write interface configured to write the processed fragment to the graphics memory (Col. 44, lines 51-61; Col. 112, line 64-Col. 113, line 4), as shown in Figure 9. This would be obvious for the same reasons given in the rejection for Claim 1.

17. With regard to Claim 13, Duluk 1 describes that the portion of a position specifies a region of fragment positions (Col. 14, lines 18-21; Col. 9, lines 2-13).

18. With regard to Claim 14, Duluk 1 describes that the read interface (1210, Figure 2) is configured to read data responsive to the position conflict status (*MMU 1210 controls access to texture memory 1213*, Col. 8, lines 59-60; *when a miss address is found, it is sent to texture*

MMU 1210, Col. 13, lines 5-6; *read miss requests are prioritized by prioritization block 2620, prioritization block 2620 sends the addresses to request queues 2621-0 and 2621-1, the addresses stored in request queues 2521-0 and 2621-1 are applied to reorder logic circuitry 2623-0 and 2623-1*, Col. 13, lines 53-67; *reorder logic 2623-0, conflict detection block 2602*, Col. 14, lines 12-21).

19. With regard to Claim 15, Duluk 1 describes that a position stored in the conflict detection unit includes at least a buffer identifier and a pair of coordinates (*tags indicate whether a texel is stored in texel prefetch buffer 1216, and the location of the texel in the buffer*, Col. 8, lines 54-58; *read miss control circuitry 2600 receives a read miss request from the miss logic when the tag mechanism determines that the desired information is not contained in texel prefetch buffer 1216, reorder logic 2623-0 and 2623-1*, Col. 13, lines 46-67; Col. 14, lines 12-40).

20. With regard to Claim 16, Duluk 1 describes that the fragment processing unit further includes a data cache configured to store data entries, each data entry associated with a position in a buffer (*when texels are moved into texel prefetch buffer 1216, a corresponding tag is created in one of the eight prefetch buffer tag blocks 1220-0 through 1220-7*, Col. 12, lines 3-7, *this mapping ensures that all eight tags can be accessed in each cycle, and that texture information is evenly distributed in the caches*, Col. 12, lines 35-37; Col. 11, lines 24-26).

21. Claims 2, 3, 5, 6, and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duluk 1 (US006288730B1) and Duluk 2 (US006771264B1) in view of Holmes (US006490635B1).

22. With regard to Claim 2, Duluk 1 and Duluk 2 are relied upon for the teachings as discussed above relative to Claim 1. Duluk 1 describes that the tracking comprises entering the location associated with the pending write in a conflict detection unit (Col. 14, lines 12-27).

However, Duluk 1 and Duluk 2 do not specifically teach updating the conflict detection unit when the pending write to the location is completed. However, Holmes describes that the tracking comprises entering the location associated with the pending write in a conflict detection unit (*conflict detection method comprises the steps of decoding a first command, where the first command is a queued read or a write, and reading an associated first logical block address and first block count (LBA), where the first LBA and the first block count define a first address range*, Col. 3, lines 2-6); and updating the conflict detection unit when the pending write to the location is completed (*the conflict detection method also comprises the step of clearing the conflict flag upon completion of the first command*, Col. 3, lines 53-56).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Duluk 1 and Duluk 2 to include updating the conflict detection unit when the pending write to the location is completed as suggested by Holmes because Holmes suggests that this is needed so that the conflict detection unit knows when the pending write to the location is completed so that the conflict detection unit knows when another read or write can be performed at that location (Col. 3, lines 53-56; Col. 5, lines 62-64).

23. With regard to Claim 3, Duluk 1 describes that the tracking comprises entering a region containing the location associated with the pending write in a conflict detection unit (Col. 14, lines 12-40).

However, Duluk 1 does not specifically teach updating the conflict detection unit when the pending write to the location is completed. However, Holmes describes that the tracking comprises entering a region containing the location associated with the pending write in a conflict detection unit (Col. 3, lines 2-6); and updating the conflict detection unit when the pending write to the location is completed (Col. 3, lines 53-56). This would be obvious for the same reasons given in the rejection for Claim 2.

24. With regard to Claim 5, Duluk 1 does not specifically teach invalidating the entry in the data cache associated with the pending write to the location in the buffer. However, Holmes describes invalidating the entry in the data cache associated with the pending write to the location in the buffer (*valid flag 550 indicates that the tag value of the corresponding entry is valid, i.e. is associated with a pending command and cannot be reused until the pending command completes*, Col. 5, lines 14-17).

It would be obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Duluk 1 to include invalidating the entry in the data cache associated with the pending write to the location in the buffer as suggested by Holmes because Holmes suggests that this is needed so that the conflict detection unit can detect at where conflicts could potentially occur and avoid the conflicts (Col. 3, lines 14-16).

25. With regard to Claim 6, Duluk 1 does not specifically teach updating the entry in the data cache when the pending write to the location is completed. However, Holmes describes updating the entry in the data cache when the pending write to the location is completed (*clearing the conflict flag upon completion of the first command*, Col. 3, lines 53-56; *cache 420 temporarily stores read data from the storage disks to be transferred to the host and write data received from the host to be written to the storage disks*, Col. 4, lines 34-37; *microprocessor 410 utilizes the queued command RAM 500 in conjunction with the command FIFO 470 for queued command handling*, Col. 5, lines 45-47, *if a conflict flag is clear, the microprocessor does not restrict reordering for the corresponding command*, Col. 5, lines 62-64).

It would be obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Duluk 1 to include updating the entry in the data cache when the pending write to the location is completed as suggested by Holmes because Holmes suggests that after the pending write to the location is completed, there will no longer be a conflict, so then updating the entry in the data cache is allowed (Col. 3, lines 53-56; Col. 5, lines 45-67).

26. With regard to Claim 17, Duluk 1 does not specifically teach that the data cache is configured to invalidate a data entry associated with a position in a buffer when a write is pending for the position in the buffer, producing an invalid data entry. However, Holmes describes that the data cache is configured to invalidate a data entry associated with a position in a buffer when a write is pending for the position in the buffer, producing an invalid data entry

(Col. 5, lines 14-17). This would be obvious for the same reasons given in the rejection for Claim 5.

27. With regard to Claim 18, Duluk 1 describes that the data cache is configured to read data from the position in the buffer and store the data read in the data entry associated with the position in the buffer, so there is a write pending for the position in the buffer for this data entry (*when texels are moved into texel prefetch buffer 1216, a corresponding tag is created in one of the eight prefetch buffer tag blocks 1220-0 through 1220-7*, Col. 12, lines 3-7, *this mapping ensures that all eight tags can be accessed in each cycle, and that texture information is evenly distributed in the caches*, Col. 12, lines 35-37; Col. 11, lines 24-26; *if there is a cache miss, when a fragment and texture map are encountered for the first time, that texture map is retrieved and stored in the cache*, Col. 16, lines 16-19; Col. 13, lines 45-67; Col. 14, lines 12-27).

However, Duluk 1 does not specifically teach that the data entry is invalid when a write it pending for the position in the buffer. However, Holmes describes that the data entry is invalid when a write it pending for the position in the buffer (Col. 5, lines 14-17). This would be obvious for the same reasons given in the rejection for Claim 5.

28. With regard to Claim 19, Duluk 1 does not specifically teach that the data cache is configured to update the entry in the data cache when the write to the position in the buffer is completed. However, Holmes describes that the data cache is configured to update the entry in the data cache when the write to the position in the buffer is completed (Col. 3, lines 53-56; Col.

5, lines 45-67; Col. 4, lines 34-47). This would be obvious for the same reasons given in the rejection for Claim 6.

29. Claims 8, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duluk 1 (US006288730B1) in view of Wood (US006204856B1).

30. With regard to Claim 8, Duluk 1 is relied upon for the teachings as discussed above relative to Claim 7.

However, Duluk 1 does not teach that the fragment program performs depth buffering prior to shading. However, Wood describes that the fragment program performs depth buffering prior to shading (Col. 1, lines 22-24; Col. 9, lines 64-67; Col. 12, lines 1-6).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Duluk 1 so that the fragment program performs depth buffering prior to shading as suggested by Wood because Wood suggests the advantage of reducing the number of attributes to be calculated (Col. 1, lines 22-24; Col. 9, lines 64-67; Col. 12, lines 1-6).

31. With regard to Claim 10, Duluk 1 describes processing another fragment as specified by the fragment program while waiting for the write to complete (Col. 10, lines 48-52).

32. With regard to Claim 11, Duluk 1 describes that the buffer is one of several buffers stored in graphics memory (Col. 9, lines 21-29).

33. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Duluk 1 (US006288730B1) and Wood (US006204856B1) in view of Isard (US 20040207623A1).

Duluk 1 and Wood are relied upon for the teachings as discussed above relative to Claim 8.

However, Duluk 1 and Wood do not teach that the fragment program performs depth peeling. However, Isard describes that the fragment program performs depth peeling [0017, 0055].

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Duluk 1 and Wood so that the fragment program performs depth peeling as suggested by Isard because Isard suggests that depth peeling is needed to render shadows cast by transparent objects [0055].

34. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Duluk 1 (US006288730B1) and Duluk 2 (US006771264B1) in view of Aglietti (US006567907B1).

Duluk 1 and Duluk 2 are relied upon for the teachings as discussed above relative to Claim 15.

However, Duluk 1 and Duluk 2 do not teach that the conflict detection unit includes a hash unit. However, Aglietti describes that the conflict detection unit includes a hash unit (30, Figure 1; Col. 3, lines 4-12).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Duluk 1 and Duluk 2 so that the conflict detection unit includes a hash unit as suggested by Aglietti because Aglietti suggests that the hash unit enables

a reduction in the complexity of circuitry that is implemented in the buffer and increases the speed of reading the buffer (Col. 2, lines 51-57).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Kee M. Tung
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